PIC18 Q41 Family Product Brief

Introduction

The PIC18 Q41 microcontroller family is available in 14/20-pin devices for real-time control and sensor applications. This analog-focused family features a 12-bit ADC with Computation (ADC^2) automating Capacitive Voltage Divider (CVD) techniques for advanced capacitive touch sensing, averaging, filtering, oversampling and threshold comparison, two 8-bit DAC modules and an Operational Amplifier. The family showcases a 16-bit PWM module which provides dual independent outputs on the same time base. Additional features include vectored interrupt controller with fixed latency for handling interrupts, system bus arbiter, Direct Memory Access (DMA) capabilities, UART with support for asynchronous, DMX, DALI and LIN protocols, SPI, I^2C, and a programmable 32-bit CRC with Memory Scan. This family also includes memory features such as Memory Access Partition (MAP) to support users in data protection and bootloader applications, and Device Information Area (DIA), which stores factory calibration values to help improve temperature sensor accuracy.

PIC18 Q41 Family Types

Table 1. Devices included in this family

Device	Program Memory Flash (bytes)	Data SRAM (bytes)	Data EEPROM (bytes)	Memory Access Partition/ Device Information Area	I/O Pins/ Peripheral Pin Select	8-Bit Timer with HLT/ 16-Bit Timers	16-Bit Dual PWM/ CCP	Complimentary Waveform Generator	Signal Measurement Timer	Numerically Controlled Oscillator	Configurable Logic Cell	12-Bit ADC^2 (channels)	8-Bit DAC	Operational Amplifier	Comparator/ Zero-Cross Detect	High-Low Voltage Detect	SPI / I^2C	UART/ UART with Protocol Support	Direct Memory Access (DMA)	Windowed Watchdog Timer	32-Bit CRC with Scanner	Vectored Interrupts	Peripheral Module Disable	Temperature Indicator
PIC18F04Q41	16k	1024	512	Y/Y	12/Y	2/3	3/1	1	1	1	4	11	2	1	2/1	1	2/1	2/1	4	Y	Y	Y	Y	Y
PIC18F05Q41	32k	2048	512	Y/Y	12/Y	2/3	3/1	1	1	1	4	11	2	1	2/1	1	2/1	2/1	4	Y	Y	Y	Y	Y
PIC18F06Q41	64k	4096	512	Y/Y	12/Y	2/3	3/1	1	1	1	4	11	2	1	2/1	1	2/1	2/1	4	Y	Y	Y	Y	Y
PIC18F14Q41	16k	1024	512	Y/Y	18/Y	2/3	3/1	1	1	1	4	17	2	1	2/1	1	2/1	2/1	4	Y	Y	Y	Y	Y
PIC18F15Q41	32k	2048	512	Y/Y	18/Y	2/3	3/1	1	1	1	4	17	2	1	2/1	1	2/1	2/1	4	Y	Y	Y	Y	Y
PIC18F16Q41	64k	4096	512	Y/Y	18/Y	2/3	3/1	1	1	1	4	17	2	1	2/1	1	2/1	2/1	4	Y	Y	Y	Y	Y

Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC – 64 MHz clock input
  - 62.5 ns minimum instruction cycle
- Four Direct Memory Access (DMA) Controllers:
  - Data transfers to SFR/GPR spaces from either Program Flash Memory, Data EEPROM or SFR/GPR spaces
  - User programmable source and destination sizes
  - Hardware and software triggered data transfers
- Vectored Interrupt Capability:

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  - Selectable high/low priority
  - Fixed interrupt latency of three instruction cycles
  - Programmable vector table base address
  - Backwards compatible with previous interrupt capabilities
- 128-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Watchdog Reset on too long or too short interval between watchdog clear events
  - Variable prescaler selection
  - Variable window size selection

Memory

- Up to 64 KB of Program Flash Memory
- Up to 4 KB of Data SRAM Memory
- 512 Bytes Data EEPROM
- Memory Access Partition: The Program Flash Memory can be partitioned into:
  - Application Block
  - Boot Block
  - Storage Area Flash (SAF) Block
- Programmable Code Protection and Write Protection
- Device Information Area (DIA) Stores:
  - Temperature indicator factory calibrated data
  - Fixed Voltage Reference measurement data
  - Microchip unique identifier
- Device Characteristics Information (DCI) Area Stores:
  - Program/erase row sizes
  - Pin count details
  - EEPROM size
- Direct, Indirect and Relative Addressing modes

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 5.5V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Functionality

- Doze: CPU and Peripherals Running at Different Cycle Rates (typically CPU is lower)
- Idle: CPU Halted While Peripherals Operate
- Sleep: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware module to minimize active power consumption of unused peripherals

- Low-Power Mode Features:
  - Sleep: < 1µA typical @ 3V
  - Operating Current:
    - 48µA @ 32 kHz, 3V, typical

Digital Peripherals

- Three 16-Bit Pulse-Width Modulators (PWM):
  - Dual outputs for each PWM module
  - Integrated 16-bit timer/counter
  - Double-buffered user registers for duty cycles
  - Right/Left/Center/Variable aligned modes of operation
  - Multiple clock and Reset signal selections
- Three 16-Bit Timers (TMR0/1/3)
- Two 8-Bit Timers (TMR2/4) with Hardware Limit Timer (HLT)
- Four Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic
- One Complimentary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
  - Programmable dead band
  - Fault-shutdown input
- One Capture/Compare/PWM (CCP) module:
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- One Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input clock up to 64 MHz
- Signal Measurement Timer (SMT):
  - 24-bit timer/counter with prescaler
  - Several modes of operation like Time-of-Flight, Period and Duty Cycle measurement etc.
- Data Signal Modulator (DSM):
  - Multiplex two carrier clocks, with glitch prevention feature
  - Multiple sources for each carrier
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate 32-bit CRC over any portion of Program Flash Memory
- Three UART modules:
  - One module (UART1) supports LIN master and slave, DMX mode, DALI gear and device protocols
  - Asynchronous UART, RS-232, RS-485 compatible
  - Automatic and user timed BREAK period generation
  - Automatic checksums
  - Programmable 1, 1.5, and two Stop bits
  - Wake-up on BREAK reception
  - DMA compatible
- Two SPI modules:
  - Configurable length bytes
  - Arbitrary length data packets

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  - Transmit-without-receive and receive-without-transmit option
  - Transfer byte counter
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
- One I^2C module, SMBus, PMBus™ Compatible:
  - 7-bit and 10-bit addressing modes with address masking modes
  - Dedicated address, transmit and receive buffers and DMA capabilities
  - Bus collision detection with arbitration
  - Bus time-out detection and handling
  - I^2C, SMBus 2.0 and SMBus 3.0, and 1.8V input level selections
  - Multi-Master mode, including self-addressing
- Device I/O Port Features:
  - 12 I/O pins (PIC18F04/05/06Q41)
  - 18 I/O pins (PIC18F14/15/16Q41)
  - Individually programmable I/O direction, open-drain, slew rate and weak pull-up control
  - Interrupt-on-change on most pins
  - Three programmable external interrupt pins
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

Analog Peripherals

- Analog-to-Digital Converter with Computation (ADC^2):
  - Up to 17 external channels
  - Automated math functions on input signals:
    - Averaging, filter calculations, oversampling and threshold comparison
  - Operates in Sleep
  - Four internal analog channels
  - Hardware Capacitive Voltage Divider (CVD) Support:
    - Adjustable sample and hold capacitor array
    - Guard ring digital output drive
    - Automates touch sampling and reduces software size and CPU usage when touch or proximity sensing is required
- Two 8-Bit Digital-to-Analog Converters (DAC):
  - Buffered output available on two I/O pins
  - Internal connections to ADC and Comparators
- Two Comparators (CMP):
  - Four external inputs
  - Configurable output polarity
  - External output via Peripheral Pin Select
- One Operational Amplifier:
  - 6 MHz Gain Bandwidth
  - Programmable Gain
  - Internal Gain Resistor Ladder
- Zero-Cross Detect (ZCD):
  - Detect when AC signal on pin crosses ground
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels
  - Internal connections to ADC, Comparator and DAC

Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 64 MHz
  - ±1% at calibration
  - Active Clock Tuning of HFINTOSC for better accuracy
- 32 kHz Low-Power Internal Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External High-Frequency Oscillator Block:
  - Three crystal/resonator modes
  - Digital Clock Input mode
  - 4x PLL with external sources
- Fail-Safe Clock Monitor:
  - Allows for operational recovery if external clock stops
- Oscillator Start-up Timer (OST):
  - Ensures stability of crystal oscillator sources

Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip

Packages

Table 2. Packages

Device	14-Pin TSSOP	14-Pin SOIC	16-Pin VQFN	20-Pin PDIP	20-Pin SOIC	20-Pin SSOP	20-Pin VQFN
PIC18F04Q41	●	●	●				
PIC18F05Q41	●	●	●				
PIC18F06Q41	●						
PIC18F14Q41				●	●	●	●
PIC18F15Q41				●	●	●	●
PIC18F16Q41				●	●	●	●

Pin Diagrams

Figure 1.

14-Pin SOIC

14-Pin TSSOP

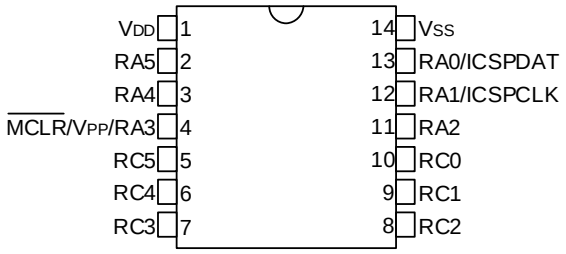
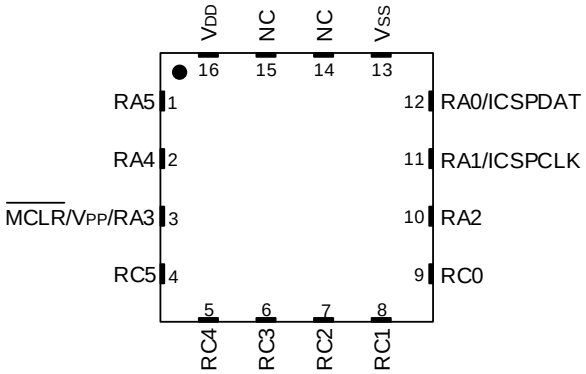


Figure 2.

16-Pin VQFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS}, however it must not be the only V_{SS} connection to the device.

Figure 3.

20-Pin PDIP

20-Pin SOIC

20-Pin SSOP

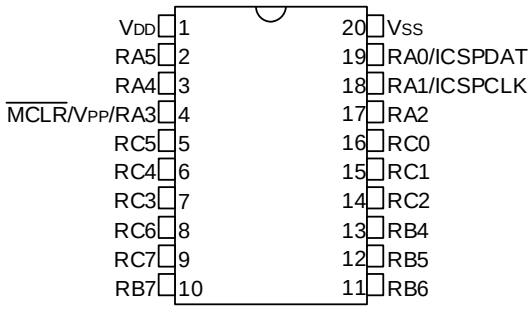


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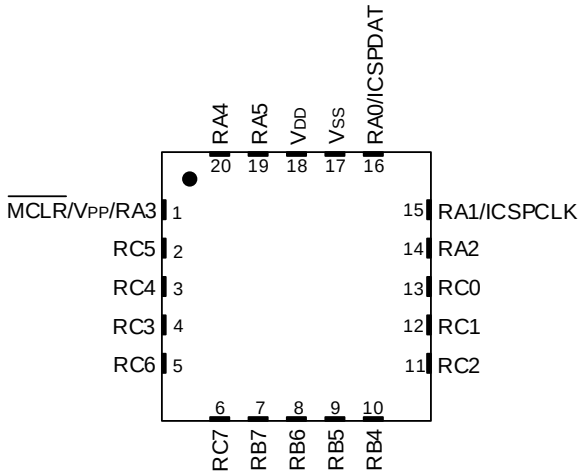
Figure 4.
20-Pin VQFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS}, however it must not be the only V_{SS} connection to the device.

Pin Allocation Tables

Table 3. 14/16-Pin Allocation Table

I/O	14-Pin SOIC/TSSOP	16-Pin VQFN	A/D	Reference	Operational Amplifier	Comparator	ZCD	Timers/SMT	16-Bit PWM/CCP	CWG	CLC	SPI	I^2C	UART	DSM	IOC	Interrupts	Basic
RA0	13	12	ANA0	DAC1OUT1	OPA1IN3+ OPA1IN3-	C1IN0+	—	—	—	—	—	SS2(1)	—	—	—	IOCA0	—	ICDDAT ICSPDAT
RA1	12	11	ANA1	VREF+ (ADC) VREF+ (DAC1) VREF+ (DAC2)	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	MDSRC(1)	IOCA1	—	ICDCLK ICSPCLK
RA2	11	10	ANA2	VREF- (ADC) VREF- (DAC1) VREF- (DAC2) DAC1OUT2	OPA1IN2+ OPA1IN2-	—	ZCDIN	T0CKI(1)	—	CWGIN(1)	—	—	—	—	—	IOCA2	INT0(1)	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	—	$\overline{MCLR}$ V_{PP}
RA4	3	2	ANA4	—	—	—	—	T1G(1)	—	—	CLCIN3(1)	—	—	RX3(1)	—	IOCA4	INT1(1)	CLKOUT SOSCO OSC2
RA5	2	1	ANA5	—	—	—	—	T1CKI(1) T2IN(1) SMT1WIN(1)	PWM1ERS(1)	—	—	—	—	CTS3(1)	—	IOCA5	INT2(1)	CLKIN SOSCI OSC1
RC0	10	9	ANC0	—	OPA1IN0+	C2IN0+	—	SMT1SIG(1)	—	—	—	SCK1(1)	SCL1(3,4)	—	—	IOCC0	—	—
RC1	9	8	ANC1	—	OPA1IN0-	C1IN1- C2IN1-	—	T4IN(1)	PWM2ERS(1)	—	CLCIN2(1)	SDI1(1)	SDA1(3,4)	RX2(1)	—	IOCC1	—	—
RC2	8	7	ANC2 ADACT(1)	—	OPA1OUT	C1IN2- C2IN2-	—	—	PWM3ERS(1)	—	—	—	—	CTS2(1)	MDCARL(1)	IOCC2	—	—
RC3	7	6	ANC3	—	OPA1IN1+ OPA1IN1-	C1IN3- C2IN3-	—	—	PWMIN2(1)	—	CLCIN0(1)	SS1(1)	—	—	—	IOCC3	—	—
RC4	6	5	ANC4	—	—	—	—	T3G(1)	—	—	CLCIN1(1)	SCK2(1)	—	CTS1(1)	—	IOCC4	—	—
RC5	5	4	ANC5	—	—	—	—	T3CKI(1)	CCP1IN(1) PWMIN1(1)	—	—	SDI2(1)		RX1(1)	MDCARH(1)	IOCC5	—	—
V_{DD}	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}

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I/O	14-Pin SOIC/TSSOP	16-Pin VQFN	A/D	Reference	Operational Amplifier	Comparator	ZCD	Timers/SMT	16-Bit PWM/CCP	CWG	CLC	SPI	I^2C	UART	DSM	IOC	Interrupts	Basic
OUT(2)	—	—	ADCGRDA ADCGRDB	—	C1OUT C2OUT	—	—	TMR0	PWM11 PWM12 PWM21 PWM22 PWM31 PWM32 CCP1	CWG1A CWG1B CWG1C CWG1D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	SS1 SCK1 SD01 SS2 SCK2 SDO2	SDA1 SCL1	DTR1 RTS1 TX1 DTR2 RTS2 TX2 DTR3 RTS3 TX3	DSM1	—	—	—

Note:

1. This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2. All digital output signals shown in these rows are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins are configured for I^2C logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RB1) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.
5. A 0.1 uF bypass capacitor to V_{SS} is required on the V_{DD} pin.

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Table 4. 20-Pin Allocation Table

I/O	20-Pin PDIP/SOIC/TSSOP	20-Pin VQFN	A/D	Reference	Operational Amplifier	Comparator	ZCD	Timers/SMT	16-Bit PWM/CCP	CWG	CLC	SPI	I^2C	UART	DSM	IOC	Interrupts	Basic
RA0	19	16	ANA0	DAC1OUT1	OPA1IN3+ OPA1IN3-	C1IN0+	—	—	—	—	—	—	—	—	—	IOCA0	—	ICDDAT ICSPDAT
RA1	18	15	ANA1	VREF+ (ADC) VREF+ (DAC1) VREF+ (DAC2)	—	C1IN0- C2IN0-	—	—	—	—	—	SS2(1)	—	—	MDSRC(1)	IOCA1	—	ICDCLK ICSPCLK
RA2	17	14	ANA2	VREF- (ADC) VREF- (DAC1) VREF- (DAC2) DAC1OUT2	OPA1IN2+ OPA1IN2-	—	ZCDIN	—	—	CWGIN(1)	CLCIN0(1)	—	—	—	—	IOCA2	—	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	—	$\overline{MCLR}$ V_{PP}
RA4	3	20	ANA4	—	—	—	—	T1G(1) SMT1SIG(1)	—	—	—	—	—	—	—	IOCA4	—	CLKOUT SOSCO OSC2
RA5	2	19	ANA5	—	—	—	—	T2IN(1) SMT1WIN(1)	PWM1ERS(1)	—	—	—	—	—	—	IOCA5	—	CLKIN SOSCI OSC1
RB4	13	10	ANB4	—	OPA1IN0-	—	—	—	—	—	CLCIN2(1)	SDI1(1)	SDA1(3,4)	—	—	IOCB4	—	—
RB5	12	9	ANB5	—	OPA1IN0+	—	—	—	—	—	CLCIN3(1)	SDI2(1)	—	RX1(1)	—	IOCB5	—	—
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	SCK1(1)	SCL1(3,4)	—	—	IOCB6	—	—
RB7	10	7	ANB7	—	—	—	—	—	—	—	—	SCK2(1)	—	CTS1(1)	—	IOCB7	—	—
RC0	16	13	ANC0	—	—	C2IN0+	—	—	—	—	—	—	(4)	—	—	IOCC0	INT0(1)	—
RC1	15	12	ANC1	—	—	C1IN1- C2IN1-	—	T4IN(1)	PWM2ERS(1)	—	—	—	(4)	RX2(1)	—	IOCC1	INT1(1)	—
RC2	14	11	ANC2 ADACT(1)	—	OPA1OUT	C1IN2- C2IN2-	—	—	PWM3ERS(1)	—	—	—	—	CTS2(1)	MDCARL(1)	IOCC2	INT2(1)	—
RC3	7	4	ANC3	—	OPA1IN1+ OPA1IN1-	C1IN3- C2IN3-	—	—	PWMIN2(1)	—	CLCIN1(1)	—	—	RX3(1)	—	IOCC3	—	—
RC4	6	3	ANC4	—	—	—	—	T3G(1)	—	—	—	—	—	—	—	IOCC4	—	—
RC5	5	2	ANC5	—	—	—	—	T3CKI(1) T0CKI(1)	CCP1IN(1) PWMIN1(1)	—	—	—	—	CTS3(1)	MDCARH(1)	IOCC5	—	—
RC6	8	5	ANC6	—	—	—	—	T1CKI(1)	—	—	—	SS1(1)	—	—	—	IOCC6	—	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—	IOCC7	—	—
V_{DD}	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}

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OUT(2)	—	—	ADCGRDA ADCGRDB	—	C1OUT C2OUT	—	—	TMR0	PWM11 PWM12 PWM21 PWM22 PWM31 PWM32 CCP1	CWG1A CWG1B CWG1C CWG1D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	SS1 SCK1 SD01 SS2 SCK2 SDO2	SDA1 SCL1	DTR1 RTS1 TX1 DTR2 RTS2 TX2 DTR3 RTS3 TX3	DSM1	—	—	—

Note:

1. This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2. All digital output signals shown in these rows are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
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5. A 0.1 uF bypass capacitor to V_{SS} is required on the V_{DD} pin.

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